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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,525	01/27/2004	Jae-Bon Koo	P56937	8987

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EXAMINER	
KIM, SUN M	
ART UNIT	PAPER NUMBER
2813	
MAIL DATE	DELIVERY MODE
04/14/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,525	KOO, JAE-BON	
	Examiner	Art Unit	
	SUN M. KIM	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/24/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the Applicant Amendment on October 23, 2008.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature of "a data line arranged on a same layer as the source and drain electrodes" of the driving TFT in claim 6 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

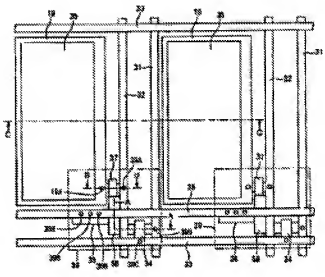
> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1, 3, and 10 – 13** are rejected under 35 U.S.C. 102(b) as being anticipated by Nozawa et al. (JP 2003-15548).

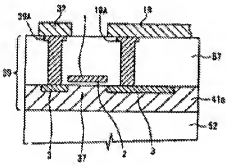
4. **In re claim 1**, Nozawa et al. shows a flat panel display, comprising (Figure 3):

- a gate line 33, a data line 31 and a power supply line 32 formed on an insulation substrate 52;
- a pixel region defined by the gate line 33, the data line 31 and the power supply line 32 (also Figure 1);
- and a pixel comprising a pixel electrode 19 arranged in the pixel region, the pixel electrode 19 being formed on the same layer as the power supply line 32, wherein the power supply line 32 is arranged on a layer different from the gate line 33 or the data line 31 (also Figure 1). In the instant case, the power supply line 32 is arranged on a layer different from the gate line 33.

【図1】



【図3】



5. **In re claim 3**, Nozawa et al. teaches that the power supply line 32 and pixel electrode 19 both being formed of the same material (Figure 3).

6. **In re claim 6**, Nozawa et al. teaches a flat panel display, comprising (Figure 3):

- a data line 31 arranged on a same layer as the source and drain electrodes 39A &19A (for instance, the same layer being substrate 52; also Figure 2 for data line 31);
- a thin film transistor comprising source and drain electrodes 39A/19A, formed on an insulation substrate 52;
- an insulation film 57 formed on the insulation substrate 52 and on the thin film transistor, the insulation film 57 being perforated by first and second contact holes exposing the source and drain electrodes 39A/19A respectively;

- a pixel electrode 19 formed on the insulation film 57 and connected to one of the source and drain electrodes through one of the first and second contact holes; and
- a power supply layer 32 formed on the insulation film and connected to the other one of the source and drain electrodes through the other one of the first and second contact holes, wherein the power supply layer 32 is arranged on a layer different from the data line 31 (also Figure 2 showing power supply layer 32 is not on data line 31).

7. **In re claim 10**, Nozawa et al. teaches flat panel display, comprising (Figures 1 and 3):

- an insulation substrate 52 divided into a plurality of pixel regions 35, each of said pixel regions being defined by a crossing of a gate line 33 and a data line 31, the insulation substrate comprising a plurality of thin film transistors, each thin film transistor 37 being arranged in corresponding ones of said plurality of pixel regions 35;
- an insulation film 57 formed on the substrate 52;
- a plurality of pixel electrodes 19 formed on the insulation film 57 and being electrically connected to corresponding ones of said plurality of thin film transistors 37 in corresponding ones of said plurality of pixel regions; and
- a power supply layer 32 formed on the insulation film 57 such that the power supply layer 32 is electrically separated from the plurality of pixel electrodes 19, said power supply layer 32 being electrically connected to each of the

plurality of thin film transistors 37 and supplying power to each of the plurality of thin film transistors 37, wherein the power supply layer 32 is arranged on a layer different from the gate line 33 or the data line 31. In the instant case, the power supply layer 32 is on a layer different from the gate line 33.

8. **In re claim 11**, Nozawa et al. teaches that the power supply layer 32 being formed in a grid shape in which corresponding ones of said plurality of pixel electrodes 19 being disposed in each grid (Figure 1). Please note that power supply layer 32 is part of a grid, therefore formed in a grid shape.

9. **In re claim 12**, Nozawa et al. teaches that the power supply layer 32 being formed in a line shape in which the power supply layer 32 is arranged between corresponding ones of said plurality of pixel electrodes 19, said power supply layer 32 being arranged in one of a row or a column (Figure 1).

10. **In re claim 13**, Nozawa et al. teaches that the power supply layer 32 having a surface electrode shape in which the power supply layer 32 is formed on a whole surface of the substrate 52 and being electrically separated from each of the plurality of pixel electrodes 19 (Figure 1).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. **Claims 4 – 5 and 7 – 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa et al. in view of Koyama (US PGPub 2003/0117083). Nozawa et al. does not teach that pixel electrode 19 is made from a material meeting the claimed characteristics, however, Koyama et al. teaches that electrode 49 can be gold (Figure 4). It would have been obvious to one having ordinary skill in the art at the time of the invention to use gold for a pixel electrode since doing so would allow for one to make a top emitting device such as shown by Koyama. Also, Nozawa et al. teaches that power supply line 32 is made from a conductive material such as metal (Paragraph 61). Koyama et al. teaches that gold is a conductive metal. It would have been obvious to one having ordinary skill in the art at the time of the invention to use gold for the power supply line of Nozawa et al. since Nozawa et al. suggests using a conductive metal and it is well known that gold is a very good conductor.

13. **In re claims 4 and 5**, the above combination would teach that both the pixde electrode and power supply line be made of gold. Gold has low resistivity and high reflectivity.

14. **In re claims 7 - 8**, the above combination would teach that both the power supply layer and pixel electrode being formed of gold. Gold has a low resistivity and a high reflectivity.

15. **In re claim 9**, the above combination teaches that the pixel electrode and the power supply layer being formed of gold. The feature of "being formed of a single film of a material" is a product by process feature. It has been held that "[E]ven though product-by-process claims are limited by and defined by the process, determination of

patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even thought he prior product was made by a different process" (In re Thorpe, 227 USPQ 964, 966, 1985, also MPEP § 2113).

16. **Claims 21 – 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa et al. in view of Komiya et al. (US Patent 6,724,149). Nozawa et al. does not teach that the power supply layer has a grid shape and surrounds a pixel region, however, Komiya et al. teaches that power supply layer 181 & 183 surrounds a pixel region 160. It would have been obvious to one having ordinary skill in the art at the time of the invention to make the power supply layer of Nozawa et al. into a grid pattern since doing so enhances the uniformity of luminescence from the pixel region (Komiya et al., Column 8, Lines 55 – 67).

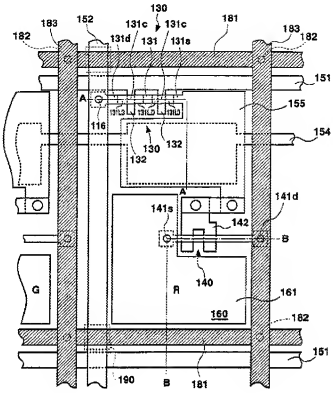


Fig. 4

Response to Arguments

17. Applicant's arguments, see Applicant Arguments, filed 10/23/08, with respect to claim 4 have been fully considered and are persuasive. The previous rejections of claims 4 – 5 and 7 - 9, which are all related, has been withdrawn.

18. With respects to the arguments presented for currently cancelled claim 2, the new amendment added to claim 1 differs from the previous subject matter of currently cancelled claim 2. Therefore, Examiner believes these arguments are now moot.

19. With respects to the arguments presented for claim 11, Applicant has not claimed that the power supply layer alone creates a grid.

20. With respects to newly added claims 21 – 23, the above rejection addresses their features.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUN M. KIM whose telephone number is (571) 270-1431. The examiner can normally be reached on Monday - Thursday 10:30 am - 8:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571) 272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sun M Kim/
Examiner, Art Unit 2813

/W. David Coleman/
Primary Examiner, Art Unit 2823